High-Density Trench DMOSFETs Employing Two Step Trench Technique and Trench Contact Structure

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Abstract - A novel process technique for fabricating trench DMOSFETs using 3 mask layers (trench, poly, metal), two step trench technique, and trench contact structure is realized in order to obtain cost-effective production capability, higher cell density, and better leakage characteristics. A unit cell with a cell pitch of 1.6 μm and a channel density of 130Mcell/in^2 are obtained. The specific on-resistance was 0.28mΩ·cm^2 with a blocking voltage of 43 V.

I. INTORDUCTION

Trench power MOSFETs are considered to be the most promising devices for use as switches in battery-pack management, DC-DC conversion, and data storage motor control. They have achieved rapid progress in the reduction of process step and on-state resistance [1-3]. Numerous advances in the cell density and fabrication process of trench technology have been reported [4-5]. Despite high cell density and low on-resistance, the reported device structures using the conventional fabrication methods (using 5~6 mask layers) have some limitation on further reducing the cell size because of process complexity.

Our previous paper [6] shows a new process technique of trench double diffused MOSFETs (DMOSFETs) to decrease process step with self-align and reliability with hydrogen annealing. For the previous method, thick silicon nitride layer of over 400 nm on the oxide should be deposited to form a space of source and pull-back regions. In this case, the thick Si_3N_4 layer can generate the stressed-induced wafer bending, causing leakage and photo litho problems.

In this paper, we propose a novel process technology with two step trench technique and trench contact structure to overcome the disadvantages of our previous technique for fabricating high density and low on-resistance trench DMOSFETs, which is also comparable with a conventional CMOS technology.

II. PROCESS DISCRIPTION

The process sequence for fabricating trench DMOSFETs using 3 mask layers was shown in Fig. 1.

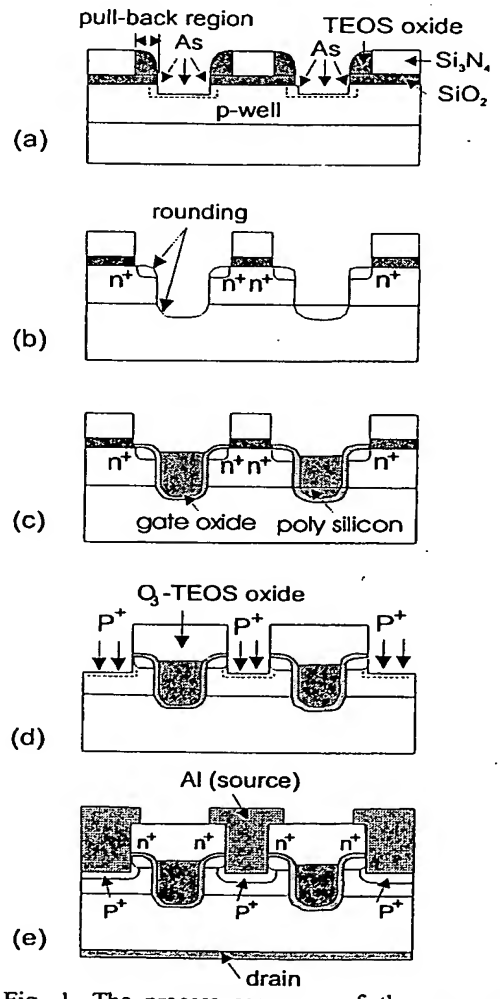

Fig. 1. The process sequence of the proposed technique

The key process steps are: a) p-well formation by blank implanting boron (~2.5E13/cm^2) and performing a drive-in diffusion, growth and deposition of SiO_2 and 2000Å of Si_3N_4 layer, oxide spacer formation by deposition and RIE etching of TEOS oxide and SiO_2 layer, 1st trench formation and removals of spacers, As ion implantation and pre-drive in, b) 2nd trench of 1.8μm formation and hydrogen annealing at 950C to form corner rounding c) growth and removal of sacrificial oxide to remove impurity distributed at the surface of the trench sidewall and improve the trench surface, gate oxide growth (50nm) on the sidewall of the trench followed by depositional of a layer of polysilicon to fill the trenches, and etch-back planarization of the doped polysilicon d) deposition and etch-back of O_3-TEOS oxide to expose the nitride layer, removal of the nitride layer and etching the silicon to implant boron ions (~3.0E15/cm^2) for p$^+$ body ohmic contact, and e) final front and backside metal deposition to form sources and drains.

The 1st trench formation and As ion implantation technique can decrease the thickness of Si_3N_4 layer until 200 nm, compared to the thickness of 400 nm used by our previous technique. The trench structure p$^+$ body contact can shrink the chip size, corresponding to the high-density and low on-resistance trench DMOSFETs.

III. EXPERIMENTAL RESULTS

Fig. 2 illustrates formation of a pair of oxide spacers by anisotropical etching of the TEOS oxide layers.

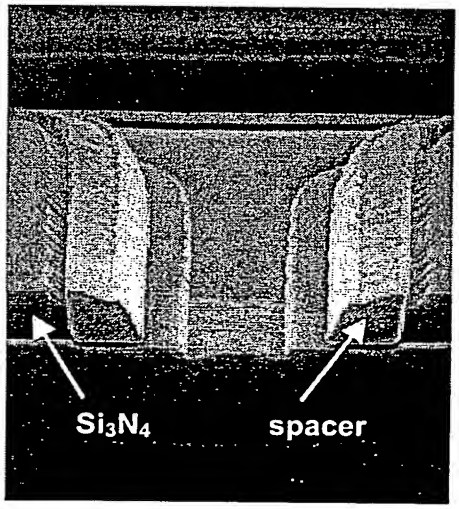

Fig. 2. SEM photograph of oxide spacer formation

The bottom width of each oxide spacer is primarily equal to the thickness (0.2μm) of the deposited Si_3N_4 layer, which only can be used to the pull-back region.

Fig. 3 shows the cross-sectional SEM photographs of the fabricated trench structure with hydrogen annealing. The corner roundings at the top and bottom of the trench with smooth surface are shown in Fig. 3. The corner rounding is formed by the pull-back and hydrogen annealing that leads to the silicon migration and crystal orientation reform from (100) to (111) [7].

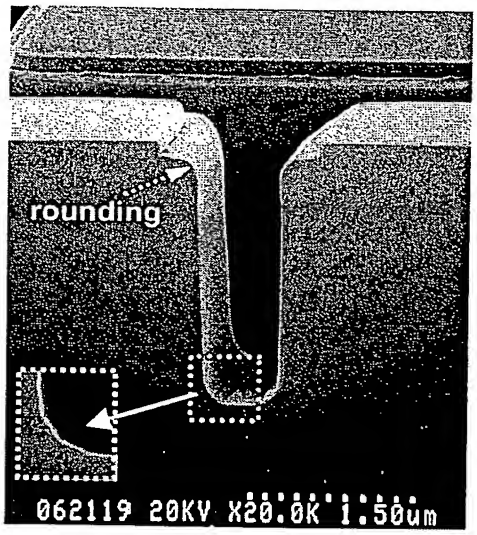

Fig. 3 SEM photograph of trench structure with hydrogen annealing

Figure 4 shows a magnified view of the reconstructed atomic configuration after atomic migration. On the surfaces, atomic rearrangement occurred on (111) plane groups. because of atomic migration, steps with 1 or 2 atomic layers were made on (111) planes. For the cubic crystal surfaces of silicon, the energy of atoms at interfaces or free surfaces depends strongly upon the efficiency of packing and hence upon the binding to neighbors.

Therefore, the more closely packed planes are expected to have the lowest values of surface tension; hence these will be the planes most likely to develop as interfaces or free surfaces. In conclusion, after the atomic migration caused by hydrogen annealing, the atomic configurations on the surfaces were composed of steps on (111) planes. This crystal orientation reform increases the oxide growth rate at the top and bottom corner of the trench, resulting in uniform oxide growth along the trench surface and higher reliability.

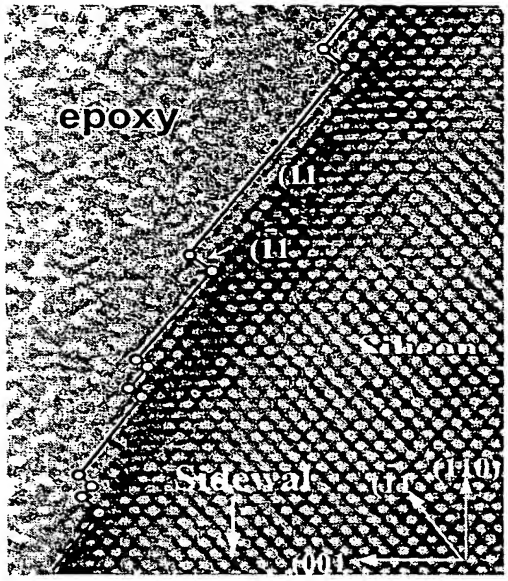

Fig. 4. Highly magnified view of a surface after atomic migration

The final structure of the trench DMOSFET with a cellular geometry fabricated by the proposed technique is seen in Fig. 5. We observed unit cells with a cell pitch of 1.6 μm, trench structure p+ body contact, and smooth corners, which are desirable to minimize the electric field stress in the gate oxide.

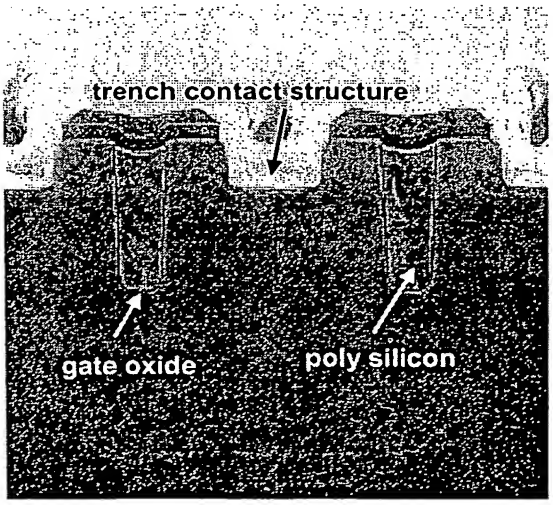

Fig. 5. Final trench structure showing gate oxide, poly silicon, and trench contact structure

By using two-step trench formation, oxide spacer, self-align technique, hydrogen annealing and three mask layers, we have successfully manufactured trench DMOSFETs with a channel density of 130Mcell/in^2 and the chip was mounted in a TO-220 package. The typical measured output current-voltage characteristics are shown in Fig 6 under the pulsed drain bias conditions.

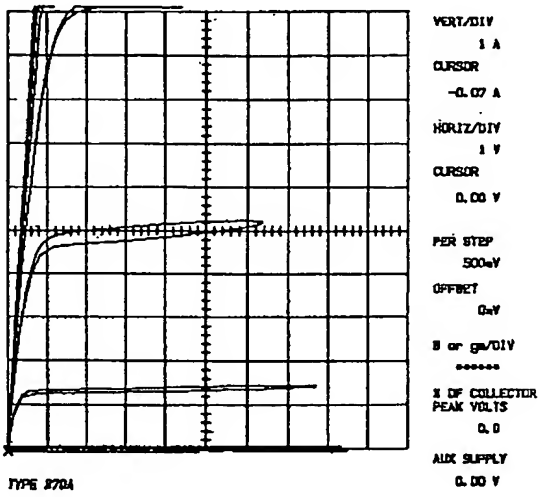

Fig. 6. The forward conduction characteristics of the proposed trench DMOFET subjected to the pulsed drain bias conditions.

The specific on-resistance is 0.28mΩ·cm^2, which is about 23 % lower than that of the device fabricated by the previous method. The thickness of the gate oxide is about 50 nm.

From the result of the plotting in Fig. 7, the I-V characteristics of the gate oxide fabricated by the proposed method is excellent with similar leakage current because of the thin Si_3N_4 layer even if the pitch size is smaller as compared with our previous device pitch.

IV. CONCLUSION

In summary, a novel process technique for fabricating trench DMOSFETs using 3 mask layers (trench, poly, metal), two step trench technique, and trench contact structure is realized in order to obtain cost-effective production capability, higher cell density, and better leakage characteristics. A unit cell with a cell pitch of 1.6 μm and a channel density of 130Mcell/in^2 are obtained. The specific on-resistance was 0.28mΩ·cm^2 with a blocking voltage of 43 V.

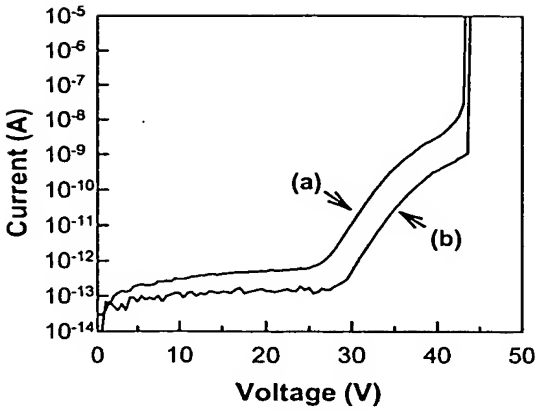

Fig. 7. I-V characteristics of trench DMOSFETs fabricated (a) previously and (b) presently under gate to drain bias condition

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